

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 depicts a schematic view of a conventional trench DMOS transistor and a bus structure thereof.

[0016] FIGS. 2A and 2B depict schematic views of a lithographic process and an etching process for forming a polysilicon bus in accordance with the bus structure shown in FIG. 1.

[0017] FIG. 3 depicts a schematic view of the formation of micro trenches in the gate oxide layer while etching the polysilicon material to form the polysilicon bus of FIG. 1.

[0018] FIG. 4 depicts a schematic view of a trench transistor and a bus structure in accordance with an embodiment of the present invention.

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[0019] FIGS. 5A through 5^E depict a sequence of steps for forming a trench transistor and a bus structure in accordance with an embodiment of the present invention.

[0020] FIG. 6 depicts a schematic view of another prior trench transistor and a bus structure.

15 DETAILED DESCRIPTION OF THE INVENTION

[0021] FIG. 4 illustrates a trench DMOS device in accordance with an embodiment of the present invention. The trench DMOS device comprises a device region 201 and a bus region 202 formed on a silicon substrate 100 overlaid by an epitaxial layer 200. The epitaxial layer 200 is doped with N dopants, and the silicon substrate 100 is doped with N+ dopants.

[0022] The device region 201 comprises a P substrate (or body) 211 of the device region formed in the epitaxial layer 200 and extending to the surface of the epitaxial layer 200. A plurality of DMOS transistors is formed in the substrate 211 of the device region. The DMOS transistor comprises, at least, two DMOS source regions 250, a DMOS trench 220, a gate oxide layer 231 of the device region, a gate polysilicon 241, a first isolation layer 261, and a source metal layer 270.

[0023] The DMOS trench 220 extends from the top surface of the epitaxial layer 200 down into the place below the substrate 211 of the device region. The gate oxide layer 231 of the device region and the gate polysilicon 241 overlie orderly the DMOS trench